PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A
MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

Nanometre Precision of Semiconductor Multilayer Growth [and Discussion]

C. T. Foxon, O. H. Hughes, D. P. Steenson and D. Lippens

Phil. Trans. R. Soc. Lond. A 1996 **354**, 2413-2423
doi: 10.1098/rsta.1996.0108

Nanometre precision of semiconductor multilayer growth

By C. T. Foxon and O. H. Hughes
Department of Physics, University of Nottingham, University Park, Nottingham NG7 2RD, UK

This article discusses the limitations imposed by the molecular beam epitaxy (MBE) growth process on the performance of double-barrier resonant tunnelling (DBRT) structures. Improved performance by optimization of the MBE process and appropriate choice of the materials system are also discussed.

1. Introduction

The performance and properties of devices, especially those involving quantum mechanical effects, depend to some extent on the quality of the growth process used to produce the basic material from which they are fabricated. In particular, the yield will inevitably depend on the uniformity of the epitaxial process and the extent of our ability to tailor heterointerfaces to the specifications laid down by the process engineer, will limit the device performance which is achieved.

Modern methods of crystal growth, such as MBE (Joyce *et al.* 1994; Hiyamizu *et al.* 1995) and metal–organic vapour phase epitaxy (MOVPE) (Kisker & Kuech 1994; Horikoshi & Minagawa 1994), have demonstrated an ability to provide high quality epitaxial material, mainly in III–V materials. These latter materials are now used extensively in commercial devices which are used in both domestic, industrial and military applications. For example, solid-state lasers are used universally in compact disc players; high electron mobility transistors find an application in satellite TV communication and modern mobile telephones include epitaxially grown heterojunction bipolar transistors. All of these require large areas of (AlGaIn)As-based materials and involve the use of low-dimensional structures/devices (LDSD). Despite strong competition from Si-based electronics, GaAs-based LDSD devices occupy a niche position in the high-frequency applications market, in particular (Fletcher 1994). The two epitaxy processes (MBE and MOVPE) have been able to provide material of a quality which is suitable for such applications, but as has been emphasized in these proceedings, so far there have been relatively few applications for devices based on resonant tunnelling structures. A question which this paper seeks to address is the extent to which the inherent limitations of the epitaxial process limit our capability in this emerging field.

In addressing this issue, we will consider three important questions, namely, what are the practical limitations of MBE for double-barrier resonant tunnelling (DBRT) structures, what are the effects of interface roughness (and how can modified growth processes improve the situation) and finally what influence does the choice of materials system have on device performance? We will limit our comments to the MBE

Phil. Trans. R. Soc. Lond. A (1996) **354**, 2413–2423
Printed in Great Britain

TEX Paper

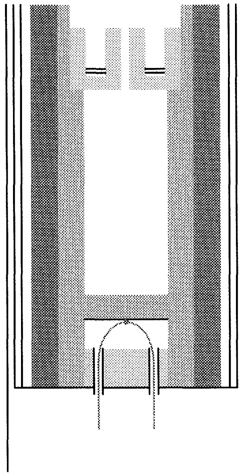


Figure 1. Schematic diagram of a Knudsen cell.

process since, for DBRT diodes, almost all the progress so far has been based on this technique. This does not, however, imply that MOVPE is any less capable of providing epitaxial material of suitable quality for this application—rather we believe that until a major market is identified, the inherent flexibility of MBE makes it the more appropriate choice for the research needs of device engineers.

2. Inherent limitations of the MBE process for DBRT structures

(a) *Thickness and compositional variations across the wafer*

The question of uniformity is of paramount importance for DBRT structures since, unlike other LDSDs, in this particular case the tunnel current through the barrier depends exponentially on the thickness and small variations have a very much stronger effect.

Early MBE systems made use of true Knudsen (equilibrium) cells of the type illustrated in figure 1. In such cells, there is a unique relationship between the pressure in the cell and its temperature. It follows that both the flux from the cell and its distribution across the wafer are constant with time. Such a cell has, however, a relatively small flux for a given temperature and is not optimized for high purity growth. To improve this situation, a non-equilibrium (Langmuir) type of source of the type shown in figure 2, has now been adopted almost universally. In this latter type, both the flux and distribution change with time as the charge becomes depleted. To make matters worse, the temperature measurement in many commercial sources is poor because the thermocouple sees the heater directly, resulting in a very inaccurate measurement of the melt temperature. Furthermore, the relationship between the flux and the temperature changes as the charge is depleted.

All molecular beam sources are Lambertian and are arranged in a ring around a source flange. It follows that there is a large variation in flux across the substrate (typically a factor of 1.5–2 across a 2 inch wafer), and that the flux distributions of the different elements also differ. To overcome this, the sample is rotated during growth but, under UHV conditions, it is impractical to rotate the substrate as quickly as once per monolayer deposited. A compromise of once per n monolayers is normal,

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

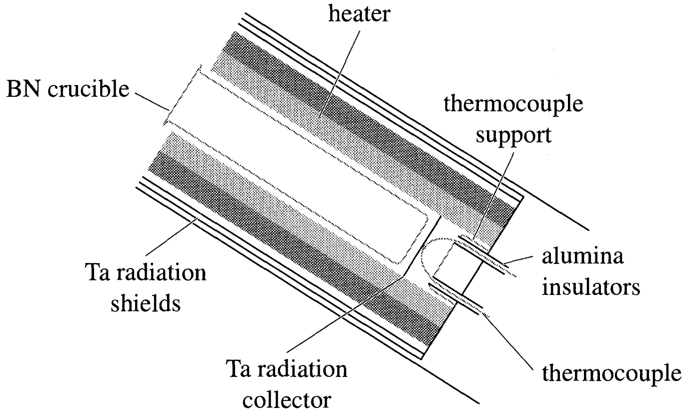


Figure 2. Schematic diagram of a typical MBE furnace—sometimes misleadingly described as a Knudsen cell or K-Cell.

where n is typically 3 or 4. This in turn gives rise to periodic variations in alloy composition at positions removed from the sample centre.

In practice, this rotation technique reduces thickness variation, for the type of source shown in figure 2, to ±15% over a 2 inch diameter wafer. This figure can be improved, by using a more conical crucible, to ±2.5%—a variation which is still less than ideal for the growth of DBRT structures. More recently, a return to a quasi-Knudsen cell arrangement has resulted in further improvement. This is achieved by using a cut-off concentric conical insert within a straight crucible inclined at the appropriate angle to the substrate. Under optimum conditions, this arrangement gives a thickness variation of only ±1.5% over a 3 inch diameter wafer. Thus by careful optimization of the MBE system and its sources, acceptable performance can be achieved.

(*b*) *Temporal variations in thickness and composition*

The fact that the source is not a true equilibrium cell means that one needs to take into account both day-to-day variations in intensity and also a systematic trend as the charge depletes. In principle, compensation for both kinds of variation can be achieved by using the *in situ* technique of reflection high-energy electron diffraction (RHEED) (Harris *et al.* 1981).

Since, in general, growth takes place on a layer-by-layer basis, the intensity of any feature in the diffraction pattern will oscillate with a period equal to the monolayer deposition time. Under appropriate conditions, this gives an absolute calibration of the group III flux arrival rate at the surface of the substrate. Further, the relative flux arrival rates of the different group III elements are an absolute measure of the alloy content of the film. This technique is used routinely as a method of calibrating the group III arrival rates and, in principle, gives very high accuracy.

In practice, the situation is somewhat different. Firstly, the RHEED oscillation measurement takes place with the sample stationary and the relationship between the value thus obtained and the average value of the actual growth rate at any point on the rotating substrate will depend upon the position of the measuring point. Only when that point is at the exact centre of rotation will the two agree precisely. Secondly, with a view to avoiding unnecessary growth on a real device, it is customary to carry out the RHEED calibrations on a monitor slice used solely for this purpose.

Removing this monitor slice and replacing it with the real slice (which may need to be brought into the growth chamber from a different location) also introduces significant errors. A final difficulty arises from the flux transients which are caused by the change in thermal load on opening or closing the shutters. In practice this transient effect may be partially compensated by pre-setting the power input to the cell at a level which produces the desired temperature after the cell has fully recovered from the opening transient.

The combined effects of all these factors results, typically, in errors in thickness of about ±5%. With care, this figure can be reduced to ±2%. Compositional errors, on the other hand, are generally smaller at ±1–2%. Again for most LDSDs, such errors are inconsequential, but for DBRT structures, they present difficulties in any manufacturing process. Even more difficulty arises, however, because the barrier regions of a typical DBRT diode are too thin to be measured by any post-growth physical method to any better accuracy than that estimated on the basis of the RHEED-determined growth rate.

(c) *Control of interface roughness in MBE*

Crystal growth is, by its very nature, a stochastic process. It follows therefore that, even though RHEED oscillations occur because of the two-dimensional nature of the growth process, growth of any particular layer starts before the previous layer is complete. Scanning tunnelling microscopy (STM) studies over large areas give a very clear idea of the nature of the problem (Sudijono *et al.* 1993). The limited migration length of the group III and group V species on the surface, at conventional growth temperatures, gives rise to inherent interface roughness. Growth clearly takes place simultaneously on several monolayers (ML) with a terrace size and shape which is influenced by growth conditions, as shown in figure 3.

A semi-quantitative measure of the diffusion length on the surface can be obtained using RHEED by studying the transition from two-dimensional nucleation and growth, to step flow at high temperatures on vicinal plane samples (Neave *et al.* 1985). When the group III diffusion length on the surface exceeds the average length of the terraces on the vicinal surface, RHEED oscillations disappear and growth takes place by step propagation across the surface. From such studies, it can be shown that, under conventional MBE growth conditions and at a typical substrate temperature of around 650 °C, the mean distance between steps on a GaAs surface is around 10–15 nm (i.e. comparable to an exciton diameter). A so-called 'normal' heterointerface, formed when a layer of (AlGa)As is grown on a GaAs layer, thus has a roughness of 2–3 MLs in the growth direction, with a terrace length between steps of about 10–15 nm. Growth is highly directional in MBE, with the preferred growth direction $[\bar{1}10]$ corresponding to the orientation of As dangling bonds—to which Ga atoms can stick on arrival.

Similar studies of the roughness and terrace size for the (AlGa)As surface, show that the 'inverted' interface (GaAs grown on (AlGa)As) is even more rough (typically 3–4 MLs) and the terrace size considerably smaller (2–3 nm). This increased roughness is due to the lower mobility of Al atoms on the surface compared with Ga atoms, which leads in turn to the inequivalence of the normal and inverted interfaces. Many *ex situ* studies by different techniques such as X-ray diffraction, transmission electron microscopy and electrical transport studies, confirm this general picture.

For DBRT structures, such roughness is of real significance since it implies that the thin barrier regions used in high current devices (typically 4–5 MLs thick), are by no

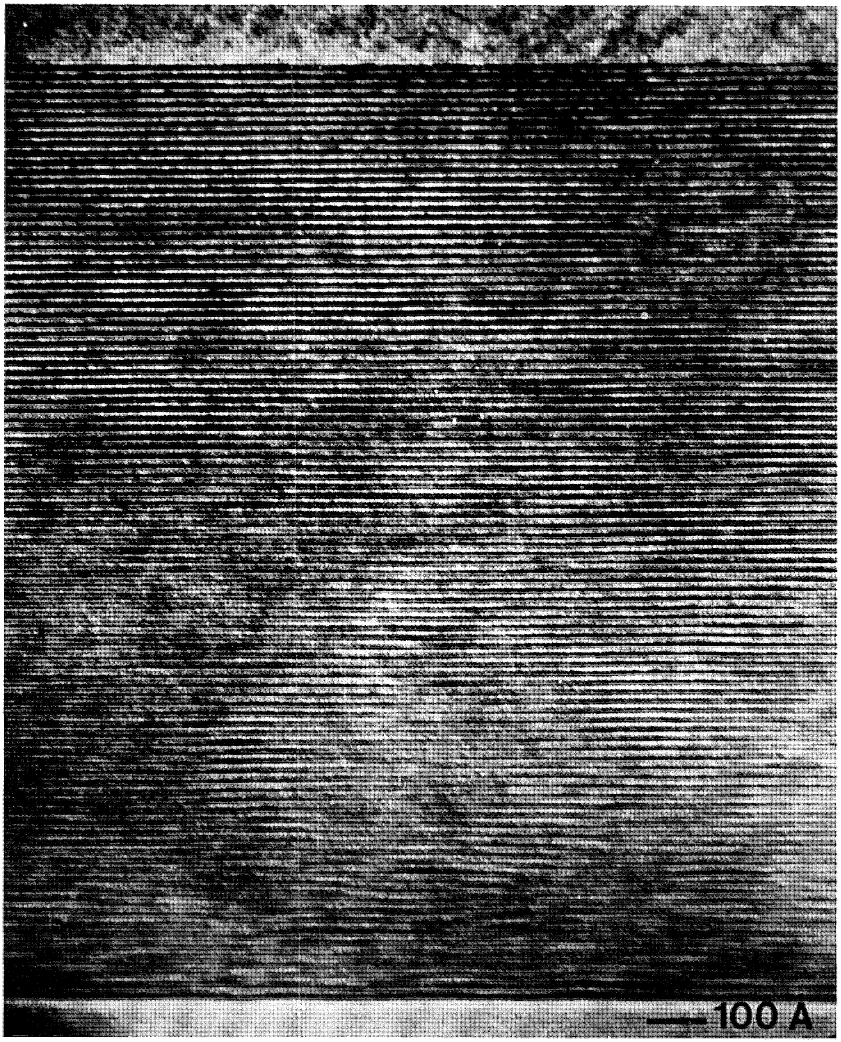


Figure 3. A large-area STM image of a layer of GaAs, illustrating the stochastic nature of the MBE growth process.

means uniform in thickness across the device. Thus the question of where the current flows under such circumstances is non-trivial and has not, so far, been addressed.

Interface quality can be improved in several ways by modified growth methods. The first method, favoured by many groups studying the optical properties of quantum wells (QWs), is to introduce a growth interrupt at the heterointerface. In the seminal work in this area, Sakaki *et al.* showed that on interrupting growth at the normal interface, the RHEED intensity recovered, but at the inverted interface no improvement was observed (Sakaki *et al.* 1985). This correlated with the observation of improved linewidth for QWs grown with interrupts at the normal interface, corresponding to the terrace length being greater than an exciton diameter, but little improvement was observed for structures grown with interruption at the inverted interface. Later work by the same group and by other authors showed that, under different conditions, similar improvements for the inverted interface can be obtained.

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

Direct experimental evidence for changes in the I–V characteristics of DBRT diodes has also been obtained (Guéret & Rossel 1991). In this case, interrupting growth at the inverted interface improved the peak current but, curiously, also increased the valley current. The width of the resonance was somewhat sharper. The same authors also demonstrated that growth on vicinal plane samples also improved the peak current, with again a corresponding small increase in the valley current.

The mechanism which gives rise to the improved performance of these diodes is not so clear, but the experiments on vicinal surfaces can be taken to suggest that the regularity of the surface steps may be a key factor. In this case, therefore, growth interruption at the inverted interface may not change the mean terrace length, but rather makes the islands more regular prior to the subsequent growth of the GaAs QWs.

Samples grown on non-(100) substrates may also be expected to have very different heterointerfaces. Studies of DBRT diodes grown on (111) surfaces show markedly different tunnelling behaviour which is thought to correlate with this difference in heterointerface quality (Harrison *et al.* 1992). The detailed interpretation of this effect is difficult, since the behaviour of tunnelling for non-ideal barriers has scarcely been investigated.

A common method used in MBE to improve heterointerfaces is to introduce a short-period superlattice (SPSL) into the buffer layers of various LDSDs. The function of the superlattice is partly to trap unwanted impurities which ride on the surface during growth (Achtnich *et al.* 1987). Large quantities of oxygen and carbon are often observed at the first inverted interface, which in the case of DBRT structures means that these impurities are located within the QW region of the device. Curiously, no-one has made a detailed study of this effect in the context of such devices, but it seems likely that pre-layers in the contact regions of the device might prove to be beneficial in reducing such contamination of the QWs.

A further consequence of introducing SPSLs is a gradual improvement in the structural quality of the heterointerfaces, as shown in figure 4. The mechanism for this progressive improvement is not established, but it is quite generally observed and is exploited in a variety of devices, especially when optical or minority carrier properties need to be optimized.

One other common occurrence in LDSDs is that structures such as SPSLs which are fabricated with purely binary layers, have better properties than those involving alloy films. This is also observed in the case of DBRT structures. For an alloy film, the stochastic nature of growth implies that on some length scale there will be a local variation of bandgap. Whether or not this influences tunnelling behaviour has yet to be established, but from an experimental point of view, binary structures are preferred. It is important to note, however, that at the heterointerface between two binary compounds (e.g. GaAs and AlAs), there inevitably exists a region of 2–3 ML which is chemically neither pure GaAs nor pure AlAs. In such regions, the material is an alloy whose composition, $(Ga_xAl_{1-x})As$, may fluctuate locally on some length scale which may be different for the growth of GaAs on AlAs from that which occurs for growth of AlAs on GaAs.

Such considerations will be especially important when both the group III and group V elements change as is the case, for example, in InAs–AlSb structures. Here there is the additional complication that the interface may be AlAs-like or InSb-like, neither of which has the same lattice parameter as that of either of the binary

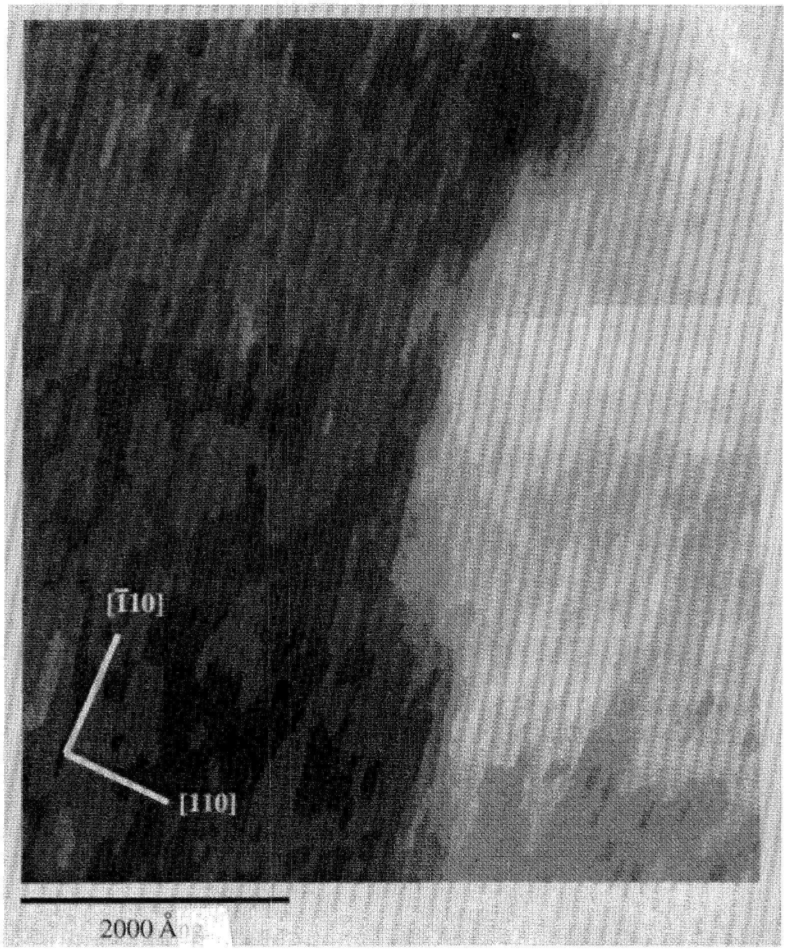


Figure 4. A TEM cross-sectional image of a GaAs–AlAs short-period superlattice.

materials. This in turn leads to compressive or tensile strain at the interfaces and the optimum termination of growth of any one material may be an important issue.

In summary, the naive picture of an atomically abrupt interface is clearly unjustified and in all DBRT structures, some departure from ideality must result. This will occur for two quite separate reasons, firstly there will be local fluctuations in the barrier thickness (and height in the case of alloy barriers) and secondly there will be local fluctuations in the QW width. The former will influence the current, especially at resonance, and the latter will affect the bias voltage at which resonance occurs. Both will give rise to a smearing of the I–V curve and reduce the peak-to-valley ratio. At present there is no clear quantitative picture of how the lack of ideality translates into inferior device performance.

(*d*) *Dopant migration during growth*

In MBE growth of III–V compounds, the commonly used n and p dopants are silicon and beryllium, respectively. More recently, carbon has been used as a p-type dopant for heterojunction bipolar transistors and magnesium for the nitrides, but the majority of DBRT structures have so far used beryllium. For DBRT structures, it is important to avoid both unintentional impurities from the ambient and the migration of dopants from the emitter and collector contacts. It has been known for some time that for both silicon and beryllium, surface segregation is observed at elevated temperature and that enhanced diffusion rates are seen at doping levels above a certain critical value (Harris *et al.* 1991). To avoid such problems, the contact regions can be grown at a reduced temperature (typically less than 500 °C) and it is normal to insert lightly doped spacer regions between the contacts and the active part of the device, especially before the growth of the DBRT structure. This has the additional advantage that electrons/holes come from a well-ordered two-dimensional region.

3. High-frequency performance

Several factors influence the high-frequency performance of DBRT structures. The optimum design of the structure includes the use of thin barrier regions to increase the peak current, optimum choice of the materials system to increase the power available and, perhaps of most critical importance, the effective series resistance of the device.

We have already noted above that the use of binary compounds, as opposed to alloys, for the barrier region brings improved device performance and the correct doping profile is clearly important in reducing the series resistance. Perhaps the most important gain in performance, however, has been obtained by using materials other than (AlGa)As. For example, at room temperature for a typical GaAs–AlAs device, a peak-to-valley current ratio (I_p/I_v) of 1.4 is observed (Sollner *et al.* 1991). For similar devices based on InGaAs, with strained AlAs barrier regions, the equivalent figure is 12 (Sollner *et al.* 1991). The improvement in this case is due mainly to a much reduced valley current. This reduction is due primarily to the larger heterojunction band offset which occurs in this materials system. The important figure of merit for device performance, however, is $\Delta I \times \Delta V$, and by going to the InAs–AlSb system, even better high-frequency behaviour is observed (Sollner *et al.* 1991). In this materials system, the highest ever reported sinusoidal oscillation frequency of 712 GHz was obtained (Brown *et al.* 1991). In this latter case, the improvements arise from increases in both ΔI and ΔV, compared with the earlier devices, and also a decrease in the contact resistance, due to the narrower bandgap InAs regions of the emitter and collector parts of the overall structure.

In the future it may be possible to further improve the performance of such devices using *in situ* contacts. Such techniques have proved valuable for other devices such as vertical surface emitting lasers (Ragay *et al.* 1993) and the technique can be applied equally well to DBRT structures.

4. Recent developments and future prospects

In the future it is possible that wide bandgap materials, such as the II–VI compounds or (AlGaIn)N, may offer even greater improvement in performance due to the larger offsets available for both conduction and valence bands. We have recently reported preliminary data for GaAs–GaN single-barrier structures which suggest that there are steps in both conduction and valence bands (Huang *et al.* 1995) and further work on DBRT structures in this materials system can be anticipated.

Other novel structures which have been studied include type II systems, where tunnelling occurs from electron states in the contact regions via hole state states in the QW region of the DBRT structure (Söderström *et al.* 1989) and also Si–SiGe devices, which have been used to probe the valence band structure in these materials (Gennser *et al.* 1991) using the method first developed for (AlGa)As (Hayden *et al.* 1991). This technique of resonant magnetotunnelling has been further developed to map the anisotropy of the hole states in novel orientation structures (Hayden *et al.* 1994).

5. Conclusions

The MBE growth process can be optimized to obtain very uniform films of constant composition over large areas. This involves optimum design of both the growth chamber and the evaporation sources. Interfaces in MBE can be influenced by appropriate modifications in the growth procedures, using techniques such as growth interruption or the use of SPSLs to improve performance. Finally, the use of novel materials systems can be exploited to further enhance performance. Given the flexibility of the MBE process, it should in the future be possible to provide high-frequency performance at higher power levels.

The authors thank Laurence Eaves, Martyn Chamberlain and Peter Main for valuable discussions during the preparation of this article.

References

Achtnich T., Burri G., Py, M. A. & Ilegems, M. 1987 *Appl. Phys. Lett.* **50**, 1730.

Brown, E. R., Söderström, J. R., Parker, C. D., Mahoney, L. J., Molvar, K. V. & McGill, T. C. 1991 *Appl. Phys. Lett.* **58**, 2291.

Fletcher, A. 1994 GaAs electronic materials and devices: a strategic study of markets, technologies and companies worldwide. *Elsevier advanced technology.* Amsterdam: Elsevier.

Gennser, U., Kesan, V. P., Syphers, D. A., Smith, T. P., Iyer, S. S. & Yang, E. S. 1991 *Phys. Rev. Lett.* **67**, 3828.

Guéret, P. & Rossel, C. 1991 NATO ASI Series B, vol. 277, p. 71.

Harris, J. J., Clegg, J. B., Beall, R. B., Castasgne, J., Woodbridge, K. & Roberts, C. 1991 *J. Cryst. Growth* **111**, 239.

Harris, J. J., Joyce, B. A. & Dobson, P. J. 1981 *Surface Sci.* **103**, L90.

Harrison, P. A., Hayden, R. K., Henini, M., Valadares, E. C., Hughes, O. H. & Eaves, L. 1992 *J. Vac. Sci. Technol.* B **10**, 2040.

Hayden, R. K., Eaves, L., Henini, M., Valadares, E. C., Kuhn, O., Maude, D. K., Portal, J. C., Takamasu, T., Miura, N. & Ekenberg, U. 1994 *Semicond. Sci. Technol.* **9**, 298.

Hayden, R. K., Maude, D. K., Eaves, L., Valadares, E. C., Henini, M., Sheard, F. W., Hughes, O. H., Portal, J. C. & Cury, L. 1991 *Phys. Rev. Lett.* **66**, 1749.

Hiyamizu, S., Shiraki, Y. & Gonda, S. (eds) 1995 *J. Cryst. Growth* **150**.

Horikoshi, Y. & Minagawa, S. 1994 *J. Cryst. Growth* **145**.

Huang, X., Cheng, T. S., Hooper, S. E., Foster, T. J., Jenkins, L. C., Wang, J., Foxon, C. T., Orton, J. W., Eaves, L. & Main, P. C. 1995 *J. Vac. Sci. Technol.* B **13**, 1582.

Joyce, B. A., Vvedensky, D. D. & Foxon, C. T. 1994 *Handbook on semiconductors* (ed. T. S. Moss), vol. 3, p. 275. Amsterdam: Elsevier.

Kisker, D. W. & Kuech, T. F. 1994 *Handbook of crystal growth* (ed. D. T. J. Hurle), vol. 3a, p. 93. Amsterdam: Elsevier.

Neave, J. H., Dobson, P. J., Joyce, B. A. & Zhang, J. 1985 *Appl. Phys. Lett.* **47**, 100.

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

Ragay, F. W., Leys, M. R. & Wolter, J. H. 1993 *Appl. Phys. Lett.* **63**, 1234.
Sakaki, H., Tanaka, M. & Yoshima, J. 1985 *Japan. J. Appl. Phys.* **24**, L417.
Sollner, T. C. L. G., Brown, E. R., Söderström, J. R., McGill, T. C., Parker, C. D. & Goodhue, W. D. 1991 Resonant tunnelling in semiconductors, physics and applications. NATO ASI Series B (ed. L. L Chang, E. E. Mendez & C. Tejedor), vol. 277, p. 487.
Sudijono, J., Johnson, M. D., Elowitz, M. B., Snyder, C. W. & Orr, B. G. 1993 *Surf. Sci.* **280**, 247.
Söderström J. R., Chow, D. H. & McGill, T. C. 1989 *Appl. Phys. Lett.* **55**, 1094.

Discussion

D. P. Steenson (*MTTG, Department of Electronic and Electrical Engineering, University of Leeds, UK*). Given a device with an area of some 20 μm^2 with, say, 5 monolayer barriers, what proportion of the current through the device could be due to terrace-type point thinning of the barriers across the active area? What is the likelihood of forming hot-spots, and how will these impinge on reliability and current–voltage variation as device sizes shrink to the point where these effects can no longer be averaged out? Is there an indication of any size below which there will be unreasonable variation between individual devices?

C. T. Foxon. It is really not possible to answer this question with any confidence since to the best of my knowledge there have been no theoretical or experimental studies of this question.

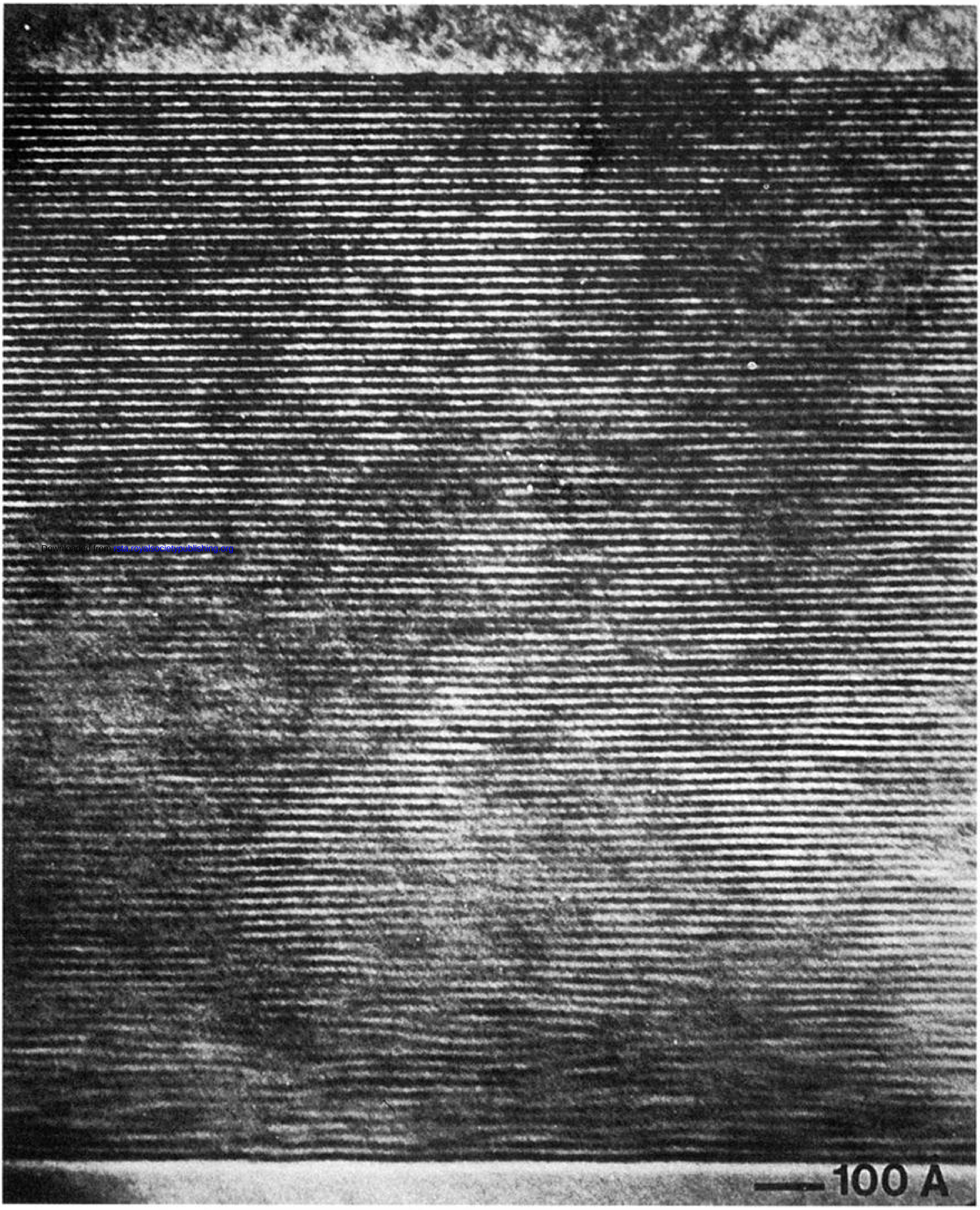
D. Lippens (*Institut d'Electronique et de Microélectronique du Nord, Université des Sciences et Technologies de Villeneuve d'Ascq, France*). Concerning the precision in the epitaxial growth of double-barrier resonant tunnelling diodes (RTD) which are able to operate at room temperature, it seems that we have to distinguish between the fluctuations in the quantum well width on one hand and in the barrier thickness on the other. For the former, it is now well known that the quantum well position is weakly dependent on the thickness of the barrier. Therefore, the uncertainty comes mainly from the width of the quantum well which determines the quantum energy position in a first approximation according to a quadratic function. Experimentally, this can be checked by means of photoluminescence (PL) measurements using resonant tunnelling structures with rather thick potential barriers (*ca.* 10 nm) in order to increase the lifetime in the well and hence the PL detected signal. On this basis, very good uniformity can be pointed out on a 2 inch wafer for structures with typically 5 nm thick quantum wells. In contrast, any variation in the barrier thickness strongly influences the current density flowing through the tunnelling structure due to the exponential variation of the quantum transmission probability as a function of the barrier width. In that case, it seems relatively difficult to address the uniformity issue by using only physical characterization tools because notably these uniformity tests have to be carried out with an ultrathin barrier typically between 1 and 2 nm for devices aimed at operating in ultrafast electronics or electro-optic applications. X-ray experiments can provide some quantitative information but require the growth of a superlattice structure. Thus it seems that only systematic study of the current-voltage characteristics could give some insight into the barrier thickness dispersion characteristics. Such a study, which often requires a high level of technology, was recently published by Hewlett Packard Laboratories with very encouraging results concerning RTDs with a peak current density which varied by less than 10% within a wafer and less than 20% from wafer to wafer (Mars *et al.* 1993).

C. T. Foxon. I agree that it is certainly true that the variation in quantum well energy will be only weakly dependent on the thickness of the barriers and that the width of the well will have the dominant influence on the resonance and that it is equally true that varations in the current will depend mainly on the thickness of the barriers. I would disagree, however, with the need to grow superlattices to extract useful information on the variation in barrier thickness from X-ray experiments. The uniformity which can be achieved over a 2 inch wafer depends on the particular arrangement of cells in the MBE system as we have indicated in this article and 'good uniformity' can be obtained in more modern machines as we have tried to indicate.

Additional references

Mars, D. E., Yang, L., Tan, M. R. & Rosner, S. J. 1993 Reproducible growth and application of AlAs–GaAs double barrier resonant tunnelling diodes. *J. Vac. Sci. Technol.* B **11**, 965.

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES



igure 3. A large-area STM image of a layer of GaAs, illustrating the stochastic nature of the MBE growth process.

PHILOSOPHICAL TRANSACTIONS OF THE ROYAL SOCIETY A MATHEMATICAL, PHYSICAL & ENGINEERING SCIENCES

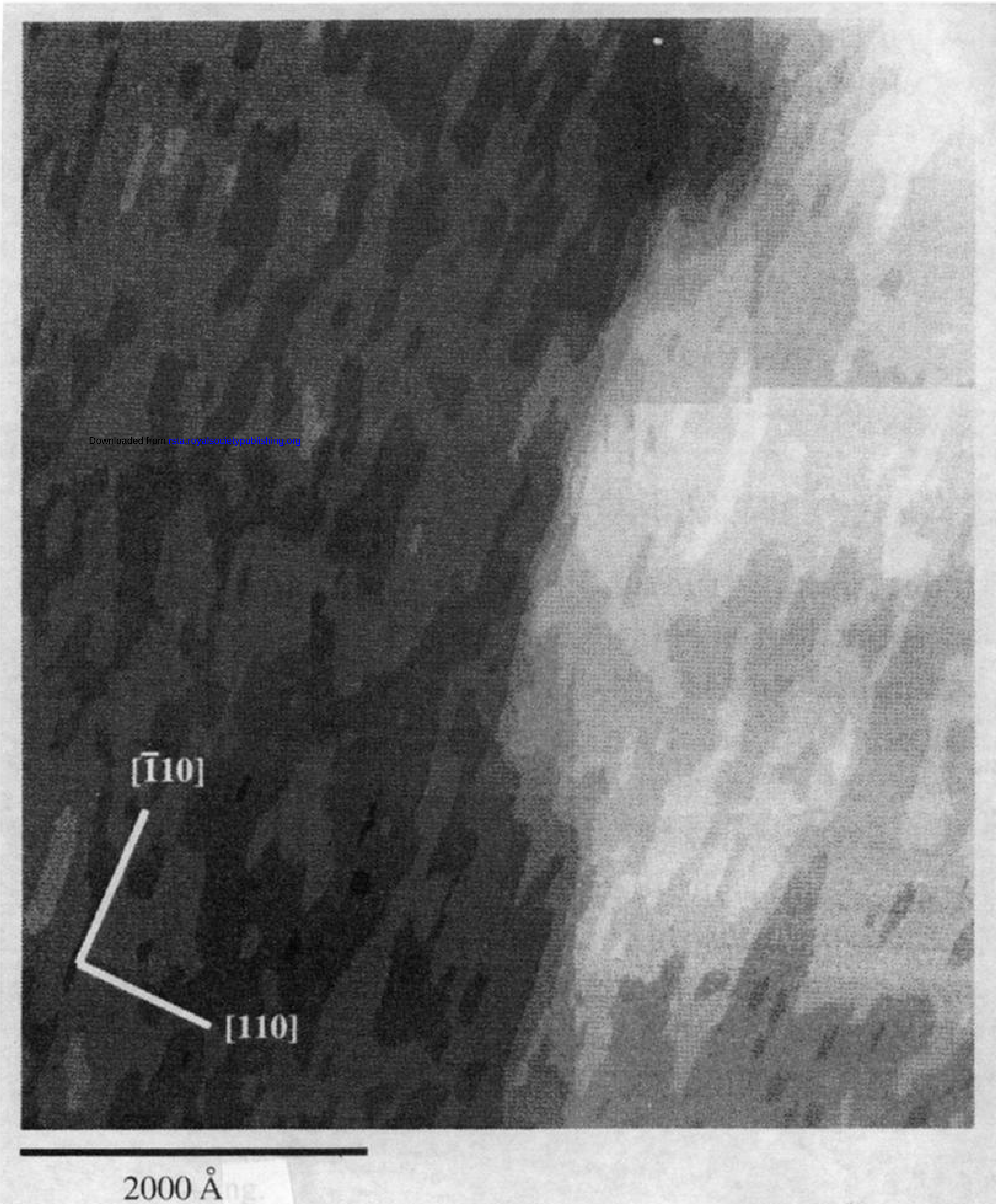


Figure 4. A TEM cross-sectional image of a GaAs–AlAs short-period superlattice.